TITLE:

COPROCESSOR ARCHITECTURE FOR CONTROL PROCESSORS USING SYNCHRONOUS LOGIC.

ABSTRACT:

A method for implementing coprocessors for control processors uses synchronous logic design method to achieve low cost and high performance in control processors. The coprocessor comprising of signed two's complement multiplication, signed divide, shift left and shift right, and normalization comprises of most of the math functions required for implementing digital signal processing algorithms. The processor coprocessor architecture uses data dependency to compute the time duration required to perform the math computation. This results in efficient implementation of DSP algorithms and eventually translates to better system level performance. The technique described to implement math computations uses a register file interface, existing instruction set, and existing legacy software development infrastructure to implement DSP systems.